

**Active**

- L1: (31807) 1 and (bitline\$1 or (bit adj. line\$1)) and (111175)
- L2: (111175) 1 and dielectric
- L3: (3876) 2 and (ROM or (read adj2 memory))
- L4: (2380) 3 and (etch\$3)
- L5: (1695) 4 and (etch\$3 near7) (dielectric or)
- L6: (1875) 4 and (etch\$3 near7) (dielectric or)
- L7: (713) 6 and (bitline\$1.clm. or (bit adj. 1))
- L8: (200) 7 and (etch\$3.near7) (dielectric or)
- L9: (200) 8 and etch\$3.clm.
- L10: (100) 9 and (3D or (three adj. dimensions))
- L11: (37) 9 and (ROM.clm. or (read adj. memory))
- L12: (0) 7 and neck\$1

Event	Line	Phase	Start	End
0	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]

[REDACTED]

[REDACTED]

Number	Country	Document ID	Issue Date	Category	Title	Current Status	Current Xref	Xref history	Inventor	File
1	US	20040617	13	Memory circuitry and method of forming memory	257/296	257/E21.64	9		Coursey, Belford T.	
2	US	20040415	69	Semiconductor integrated circuits, etc.	365/222				Goda, Akira et al.	
3	US	20040071030		UV-programmed P-type mask ROM and fabrication system	257/390	257/208			Kuo, Tung-Cheng et al.	
4	US	20040065928	10	Method of forming a mask ROM and fabrication system on chip	430/314	257/391	1		Ilu, Chien-Hung et al.	
5	US	20030232284	18	UV-programmed P-type Mask ROM and fabrication system	257/390	257/E21.61	9		Kuo, Tung-Cheng et al.	
6	US	200301002	10	Dynamic random access memory circuitry	438/241	257/E21.67	9		Coursey, Belford T.	
7	US	20030139002	13	Method of making identification code of memory circuitry	365/200	257/E21.67	2		Wen, Wen-Ying et al.	
8	US	20030128605	11	Method of making identification code of memory circuitry	438/401	257/390	1		Wen, Wen-Ying et al.	
9	US	20030109113		Dynamic random access memory circuitry	257/296	257/306			Coursey, Belford T.	
10	US	20030015745		Method of forming memory circuitry	257/309	257/305			Coursey, Belford T.	
11	US	20030123	13	Apparatus and methods for monitoring self-aligning	257/296	257/E21.64	9		Weiner, Kurt H. et al.	
12	US	20020509	11	Non-volatile memory device used for non-overlapping	257/390	257/391			Chang, Ching-Yu	
13	US	20020053708		Methods of forming dynamic random access memory	438/128	257/E21.67	9		Coursey, Belford T.	
14	US	20020025609	13	Memory Circuitry and Method	257/306	257/E21.64	9		Coursey, Belford T.	
15	US	20020024084		Dynamic Random Access Memory	365/149	257/E21.64	9		Kurth, Casey R. et al.	
16	US	20010913	28	ROM-embedded-DRAM	365/149	257/E21.64	8		Furukawa, Toshiharu et al.	
17	US	20010021122		Multi-level dram trench store utilizing two read	365/149	257/E21.09	4		Hwang, Chong Jen	
18	US	20010809	27	Method for manufacturing embedded	438/262	257/E21.67	9			
19	US	20010012215								
20	US	6699757	20040302	14						